International
IOR Rectifier

PD-60325

*i*P2005APbF

iPOWIR™ TECHNOLOGY

High Frequency Synchronous Buck Optimized LGA Power Stage

Integrated Power Semiconductors, Driver IC, & Passives

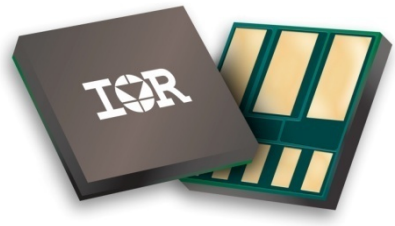
Features

- 40A Multiphase building block
- No de-rating up to T_{PCB} = 95ºC
- Optimized for low power loss
- Optimized for low EMI
- Bias supply range of 4.5V to 7.0V
- Operation up to 1.5MHz
- Bi-directional Current flow
- Under Voltage Lockout
- LGA interface
- 7.65mm x 7.65mm outline

Applications

- High Frequency, Low Profile DC-DC
- Multi-phase Architectures
- Low Duty Cycle, High Current solutions
- Microprocessor Power Supplies
- General DC/DC Converters

Package Description	Interface Connection	Standard Quantity	T & R Orientation
iP2005APbF	LGA	10	N/A
iP2005ATRPbF	LGA	2000	Figure 15

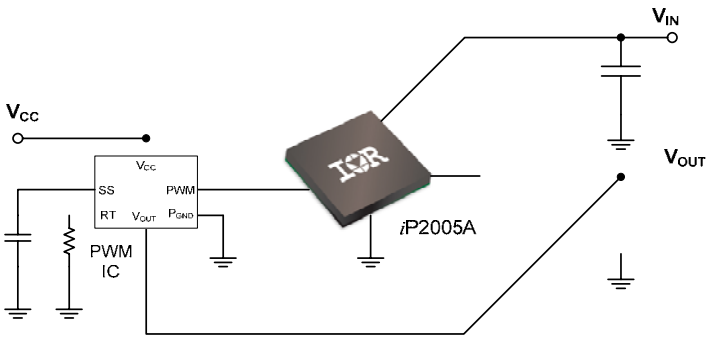


Description

The iP2005A is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 7.65mm x 7.65mm x 1.66mm power block. The additional components required for a complete multiphase converter are a PWM controller, the output inductors, and the input and output capacitors.

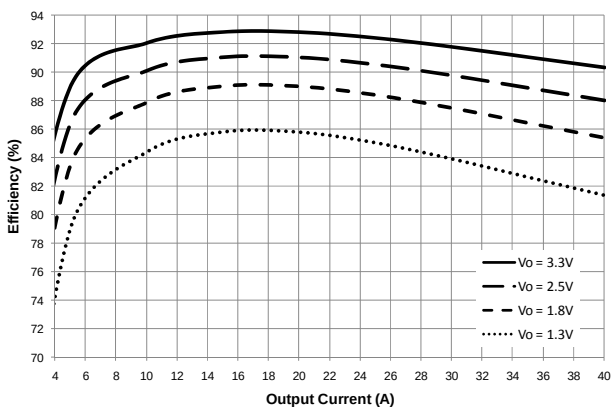
iPOWIR Technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer, and component selection.

Typical Application



iP2005A Product Efficiency

V_{IN} = 12V, F_{SW} = 1MHz, & T_{BLK} = 125ºC



ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to P_{GND})

V_{IN} to P_{GND} ……..-0.5V to 16.5V
V_{DD} to P_{GND} ……-0.5V to 7.5V
CV_{CC} to P_{GND} ……...-0.5V to 7.5V
PWM to P_{GND} ……-0.5V to VDD + 0.5V (Note 1)
ENABLE to P_{GND} ……-0.5V to VDD + 0.5V (Note 1)
Storage Temperature ……..-60ºC to 150ºC
Block Temperature ……-40ºC to 150ºC (Note 2)
ESD Rating……...JEDEC, JESD22-A114 (HBM[4KV], Class 3A)
……JEDEC, JESD22-A115 (MM[400V], Class C)
MSL Rating……..……..3
Reflow Temperature ……..260ºC Peak

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those listed in the "Recommended Operating Conditions" section of this specification is not implied.

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Voltage (V_{DD})	4.5	-	7.0	V	
Input Voltage (V_{IN})	6.5	-	13.2	V	
Output Voltage (V_{OUT})	-	-	5.5	V	
Output Current (I_{OUT})	-	-	40	A	
Switching Frequency	250	-	1500	kHz	
On Time Duty Cycle	-	-	85	%	
Minimum V_{SW} On Time	60	-	-	ns	V_{DD} = 5.0V, V_{IN} = 12V
Block Temperature (T_{BLK})	-40	-	125	ºC	(Note 2)

Electrical Specifications

These specifications apply for T_{BLK} = 0ºC to 125ºC and V_{DD} = 5.0V unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
P_{Loss}					
Power Block Losses	-	9.3	11.1	W	V_{IN} = 12V, V_{DD} = 5.0V, V_{OUT} = 1.3V, I_{OUT} = 40A, F_{SW} = 1MHz, L_{OUT} = 0.3uH, T_{BLK} = 25ºC (Note 3)
V_{DD}					
Supply Current (Stand By) (I_{Q-VDD})	-	2.2	3	mA	V_{DD} = 5.0, ENABLE = 0V
Supply Current (Operating)	-	50	65	mA	V_{IN} = 12V, ENABLE = V_{DD} = 5V, F_{SW} = 1MHz, 10% DC
CV_{CC} (LDO Output)					
Output Voltage	5.5	6.0	6.75	V	
Output Current	80	-	-	mA	
Output Capacitor	1.0	-	-	µF	Ceramic, X5R, 16V
Power-On Reset (POR)					
V_{DD} Rising	3.7	4.1	4.5	V	
Hysteresis	140	185	230	mV	V_{DD} Rising & Falling
CVCC Rising	4.2	4.6	5.0	V	
Hysteresis	165	220	275	mV	CV_{CC} Rising & Falling
ENABLE INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	Schmitt Trigger Input V_{DD} = POR to 7.0V
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull-down Impedance	-	100	-	kΩ	
Rising Propagation Delay (T_{PDH})	-	40	-	ns	
Falling Propagation Delay (T_{PDL})	-	75	-	ns	

Electrical Specifications (continued)

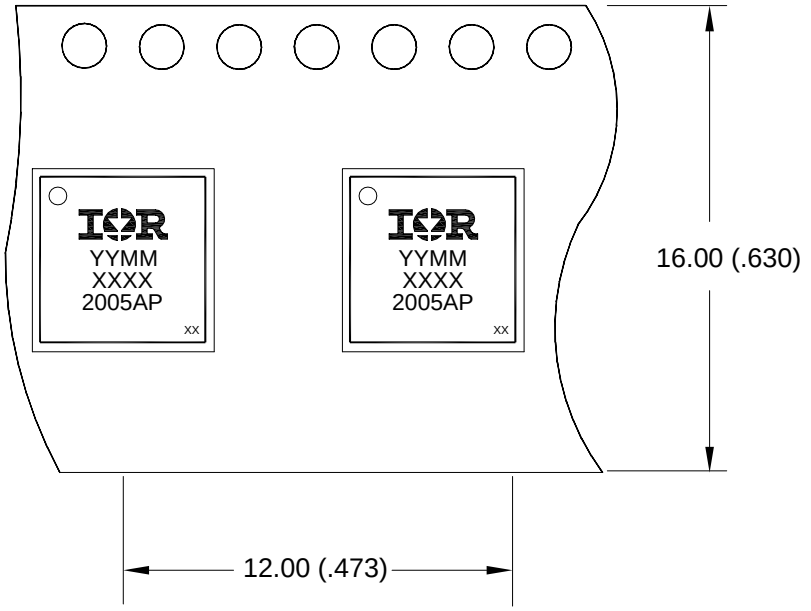
These specifications apply for T_{BLK} = 0ºC to 125ºC and V_{DD} = 5.0V unless otherwise specified.

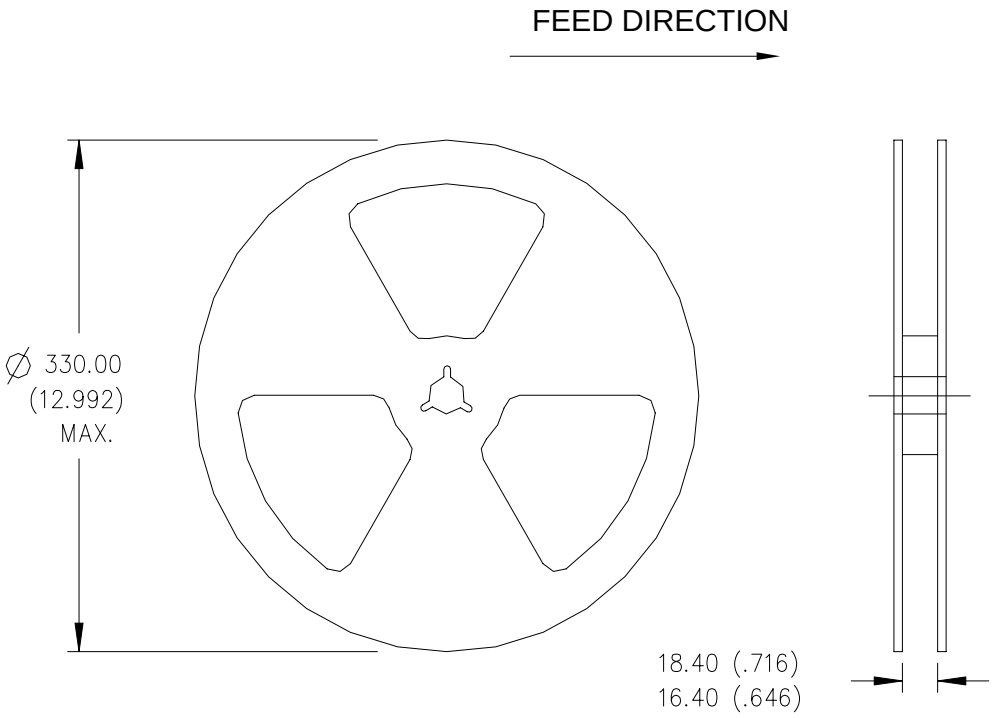
PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
PWM INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	Schmitt Trigger Input V_{DD} = POR to 7.0V (Note 4)
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull-down impedance	-	100	-	kΩ	
Rising Propagation Delay (T_{PDH})	-	60	-	ns	
Falling Propagation Delay (T_{PDL})	-	30	-	ns	

Notes:

1. Must not exceed 7.5V
2. Block Temperature (T_{BLK}) is defined as any Die temperature within the package
3. Measurement made with six 10µF (TDK C3225X5R1C106KT or equivalent) ceramic capacitors placed across VIN to PGND pins (see Figure 8)
4. Not associated with rise and fall times. Does not affect Power Loss

Tape and Reel Information





NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Figure 15 Tape and Reel Information